

## WHAT IS CLAIMED IS:

1. A testing circuit for thin film transistor display array testing, use to test the yield of thin film transistor array, comprising:

5 An array tester, providing electrical power, testing signal waveform, for analyzing, calculating, storing the testing results;

A device under test (DUT) platform, for holding the thin film transistor array, and providing control signal to the platform and the sense amplifier by the array tester;

10 A sense amplifier array, for transferring (discharge) the parasitic capacitance of the source line of the thin film transistors and integrating the charge current of the pixel storage capacitor, wherein the improvement comprising:

Said sense amplifier array is composed by a plurality of trans-impedance amplifier unit and a plurality of parasitic capacitance  
15 discharge circuit, every sense amplifier including:

A trans-impedance amplifier, is composed by an amplifier, two switches and an operation capacitor; said operation capacitor feed back the output of the amplifier to the negative input of the amplifier; a switch connecting to the output and negative input of the operational amplifier, to  
20 short circuit the operation capacitor for discharge; another switch to be the input switch, to connect or disconnect with the pixel storage capacitor; said trans-impedance amplifier forms an integrated circuit, the output is transmitted to a sampling/hold circuit via an output switch and converted to a digital signal;

25 A discharge circuit for the parasitic capacitance of the source line of the thin film transistors, composed by an amplifier, two switches and an operation capacitor; said operation capacitor feed back the output of the amplifier to the negative input of the amplifier; a switch connecting to the

output and negative input of the operational amplifier, to short circuit the operation capacitor for discharge; another switch to be the input switch, to connect or disconnect with the parasitic capacitance of the source line of the thin film transistors; a load resistance connecting the output of said  
5 operational amplifier to the ground; said discharge circuit forms a discharge circuit for the parasitic capacitance.

2. A testing circuit as recited in claim 1, wherein said thin film transistor array is liquid crystal display (LCD) panel.

3. A testing circuit as recited in claim 1, wherein said thin film  
10 transistor array is organic light emitting diode display (OLED) panel.

4. A testing circuit as recited in claim 1, wherein said thin film transistor array is LCOS (liquid crystal on silicon) panel.

5. A testing circuit as recited in claim 1, wherein said thin film transistor is amorphous thin film transistor.

15 6. A testing circuit as recited in claim 1, wherein said thin film transistor is poly-Si thin film transistor.

7. A testing circuit as recited in claim 1, wherein said thin film transistor is re-crystallized silicon thin film transistor.

20 8. A testing circuit as recited in claim 1, wherein said amplifier is operational amplifier.

9. A testing circuit as recited in claim 1, wherein said switches are control by the programmable output waveform of said array tester.

10. A testing circuit as recited in claim 1, wherein the capacitance of said operation capacitor of said trans-impedance amplifier is 1 pf to  
25 100pf.

11. A testing circuit as recited in claim 1, wherein the capacitance of said operation capacitor of said discharge circuit is greater than 10 pf.

12. A testing method for invalid pixel (invisible area) of thin film

transistor display array, comprising the steps of:

Charging the pixel storage capacitors of the  $n$ th column of the device under test to a charge voltage of  $V_s$ , then open circuit the pixel transistors after charging;

- 5 Switching ON the short circuit switches of the sense amplifiers and the discharge circuits to discharge the operation capacitors of the sense amplifiers and the discharge circuits;

Switching ON the input switches of the discharge circuits; switching OFF the short circuit switch to discharge the parasitic  
10 capacitance of the thin film transistor (transfer the charge), the transferring time is longer;

Switching ON the input switch of the sense amplifier to start operation of the sense amplifier, integrating the current from the pixel storage capacitor of column  $n$  and row  $k$ , but do not output the result;

- 15 Testing the next pixel (column  $n$  and row  $(k+1)$ ).

13. A testing method for valid pixel (visible area) of thin film transistor display array, comprising the steps of:

Charging the pixel storage capacitors of the  $n$ th column of the device under test to a charge voltage of  $V_s$ , then open circuit the pixel  
20 transistors after charging;

Switching ON the short circuit switches of the sense amplifiers and the discharge circuits to discharge the operation capacitors of the sense amplifiers and the discharge circuits;

Switching ON the input switch of the sense amplifier to start  
25 operation of the sense amplifier, integrating the current from the pixel storage capacitor of column  $n$  and row  $k$ , the integrated voltage is  $V_d$ ;

Switching ON the input switches of the discharge circuits; switching OFF the short circuit switch to discharge the parasitic

capacitance of the thin film transistor (transfer the charge), for the testing of the next pixel, the transferring time is shorter;

Testing the next pixel (column  $n$  and row  $(k+1)$ ).

14. A testing method as recited in claim 12 or 13, wherein said  
5 charging voltage  $V_s$  of the pixel capacitors is 2 Volts to 10 Volts.

15. A testing method as recited in claim 13, wherein said  
integrated voltage  $V_s$  is greater than 100 mV.

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